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LPD6803

LPD6803 is a 3 channel constant-current driver and grey-level modulate output , it uses advanced high-voltage CMOS technology, provide 3-way, designed to meet the needs of driving function in the LED lighting system, especially in the dissociation with mutual grey level in the full-colour lighting system..

LPD6803 includes serial shift register and concatenation driver circuit, grey level data shift into serial shift register in the clock, and transfer saving , it transfer to interface 3 after pulse-width modulate ,then output, serial shift register and grey-level counter can be controlled by different clock signal. In the meantime, LPD6803 driver data signal and control signal , and output next circuit.

Features:

◇ 3channel driver output, maxim current per channel is 45mA, LED light voltage can reach 12V.

◇ Output adopt In-Rush online feedback contant-current driver structure, compatible with constant-voltage module, it also can contact outside equipment and transfer to higher voltage or current output driver.

◇ Built-In LDO voltage-stabilizing circuit, voltage range is 3-8v, and have 5V stabilizing voltage output.

◇ Adopt self-add token-ring technology dual shift line, shift clock can reah 24MHz.

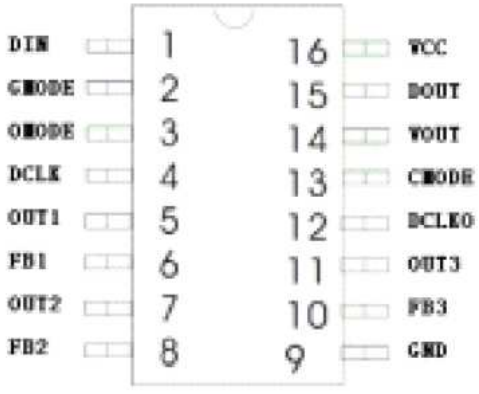
◇ Directly input grey-level data, it is transfer to 256 output with reverse-gamma regulator after inside SUPER-PWM technology, e.g, adopt built-in oscialator as greylevel clock, it support FREE-RUN module output, especially can be used in low-cost controller.

◇ Data clock signal is drived strongly to next chip to enhance level after built-in phaselock circuit.

◇ High-voltage CMOS technology, industrial design, with extra-good interference immunity

◇ With SOP16/QFN16 Pb-Free package, meet the requirement of Rohs , also can provide COB package or DIE.

Footprint of LPD6803



Function features:

- Limited parameter:

Parameter	Symbols	Range	Unit

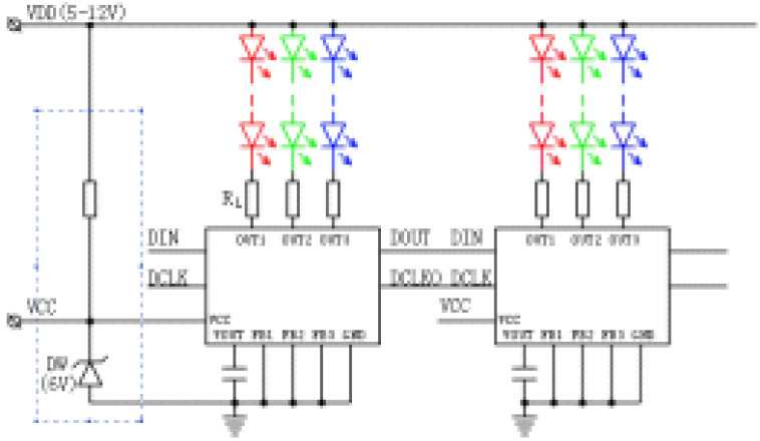
Supply voltage	VDD	3–8	V
LED light voltage	VLED	3–12	V
Data Clock Frequency	FCLK	25(compatible with grey level at 10)	MHZ
Maxim Driver Current	IOMAX	45 at constant voltage, 30 at constant current	mA
channel current error	DIO	chip inside <5%, between Chip <6%	%
power consumption	PDMAX	600	mW
Soldering Temp	TM	300(8S)	℃
Working Temp	TOP	−40 −−−+80	℃
Saving Temp	TST	−65 −−−+120	℃

Suggested working parameter:

Parameter	Symbols	Range	Unit
Supply Voltage	VDD	5–7.5	V
voltage–stabilizing output voltage	VOUT	5±5% (customer data)	V
Input Voltage	VIN	−0.4 ~ Vout+0.4	V
Data clock frequency	FCLK	0–15	MHZ
Clock high–level voltage width	TCLKH	>30	ns
Clock low–level voltage width	TCLKL	>30	ns
Data build time	TSETUP	>10	Ns
Data keep time	THOLD	>5	Ns
Power comsumption	PD	<350	mW
Working Temp	TOP	−30 ~ +60	℃

Typical application circuit:

Inside constant voltage driver (compatible with ZQL9712) mode:



This mode (OMODE=high voltage level or dangle)is suitable used in the situation which VDD not higher 12V and current on each way not huge 400mA, if VDD<7.5V, you can ignore those parts in blue dashed above chart, directly contact VDD to VCC.

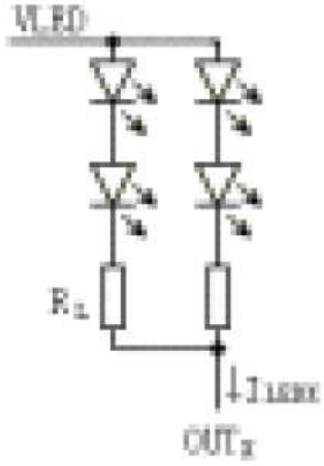
Current regulator resistance count: RL=(VDD-VLED-VOUT)/ILED

Here: RL is limit current resistance value, VDD is LED light supply voltage, VLED is LED light voltage when it breakover, VOUT is saturation voltage of the output polar to the grand(about 0.4v –0.8v), ILED is LED working current(normally no bigger 20mA)

LPD6803 has strong driver capability , in the many LED apply situation, we can adopt the contact of "First serial then parallel" (see right chart), but we must pay attention on power consumption can not exceed maxim value PDMAX:

PD=ILED1*VOUT1+ILED2*VOUT@+ILED3*VOUT3+PIC

Here : PIC is IC basic power consumption , normally not exceed 25mW.



Linking signal driver and link:

Considering of that the distance between of chips may be long long, DOUT and DCLKO

Output terminal is designed to push-pull strong drive circuit, after testing, it can drive 6meters length signal line when clock is 2M, to prevent signal echo, normally, pls serial a 50Ω resistance at DOUT and DCLKO, then output to next step.

Control circuit and software reference design:

Via set CMODE, LPD6803 grey level counter can adapt DCLK as clock(CMODE=0), Also can adapt built-in 1.2M(error ±15%)osscilator output of as clock(CMODE=1 Or dangle), prior one is normally used in those based on CPLD/FPGA high cost control system, later one is often used in low cost MCU control system.

In CMODE=1 mode, MCU write display data into chip via SPI or two GPIO interface line,
then each chip will automatically produce drive output with related duty cycle according to input grey level value, after data transfered, MCU can deal with

other
task, during this time, each LPD6803 will continue keeping original duty cycle drive output(FREE-RUN mode), till MCU send out next updated data.
Notice: after all data are input in chip on the up-edge of DCLK, it may need send more DCLK pulse (DIN=0), on principle, how many group point in the transfer link, how many related pulse need to be sent out, it is important to which later chip built-in PLL re-gernate circuit can work in gear.
To make LPD6803 produce more particularity grey level by less data, when GMODE=0/
CMODE=0, built-in SUPER-PWM can change 5 bit data into non-line 256 grade grey output, minimum open width is 1T, maxim open width is 256T (T is grey clock cycle)
When GMODE=1 or dangle , output is line 32 grade grey, minimum open width is 4T, and maxim open width is 128T.
C51 example:

```
//SDO, SCLK is data and shift output, bit variability ,nDots is light qty
// this program is only suitable in GMODE=1,CMODE=1 situation.
// first output 32 “0” start frame
SCLK=0;
SD0=0,
For (i=0;i<32;i++){SCLK=1;SCLK=0;}
// then output nDots data, here suppose each point colour are(dr,dg,db)
//dr,db,dg is red, green and blue grey level 0-31
For (i=o;i<nDots;i++)
{ SD0=1;SCLK=1;SCLK=0; //first output one “1” as start bit
//output 5 bits red data
Mask=0x10;
For (j=0; j<5; j++)
{ if (mask &dr) SD0=1;
Else SD0=0;
SCLK=1; SCLK=0;
Mask>>=1; }
// output 5 bits green data
Mask=0x10;
For (j=0; j<5; j++)
{ if(mask &dg)SD0=1;
Else SD0=0;
SCLK=1;SCLK=0;
Mask>>=1; }
```



```
//output 5bits blue data
Mask=0x10;
For (j=0; j<5; j++)
{ if(mask & db) SD0=1;
Else SD0=0;
```

```
SCLK=1;SCLK=0;
Mask>>=1; }
}
// after output all nDots data, need add nDots pulse
SD0=0;
For (i=0;i<nDots;i++){SCLK=1;SCLK=0;}
//transport data finish
Delay();
//here add some delay , or transfer to other dealings, after some time(say 1/30
second), then fresh again.
```